

FIG. 1

FIG. 2 is a block diagram of a system 200 according to one embodiment of the present invention. The system 200 includes a TLC SRAMS 8/16MB 48, a TLC Controller 26, and two parallel processing paths 28 and 30. Each path includes a parallel processing unit 50 and 54, respectively, which are connected to the TLC Controller 26. The parallel processing units 50 and 54 are each composed of two parallel processing elements 52 and 56, respectively.

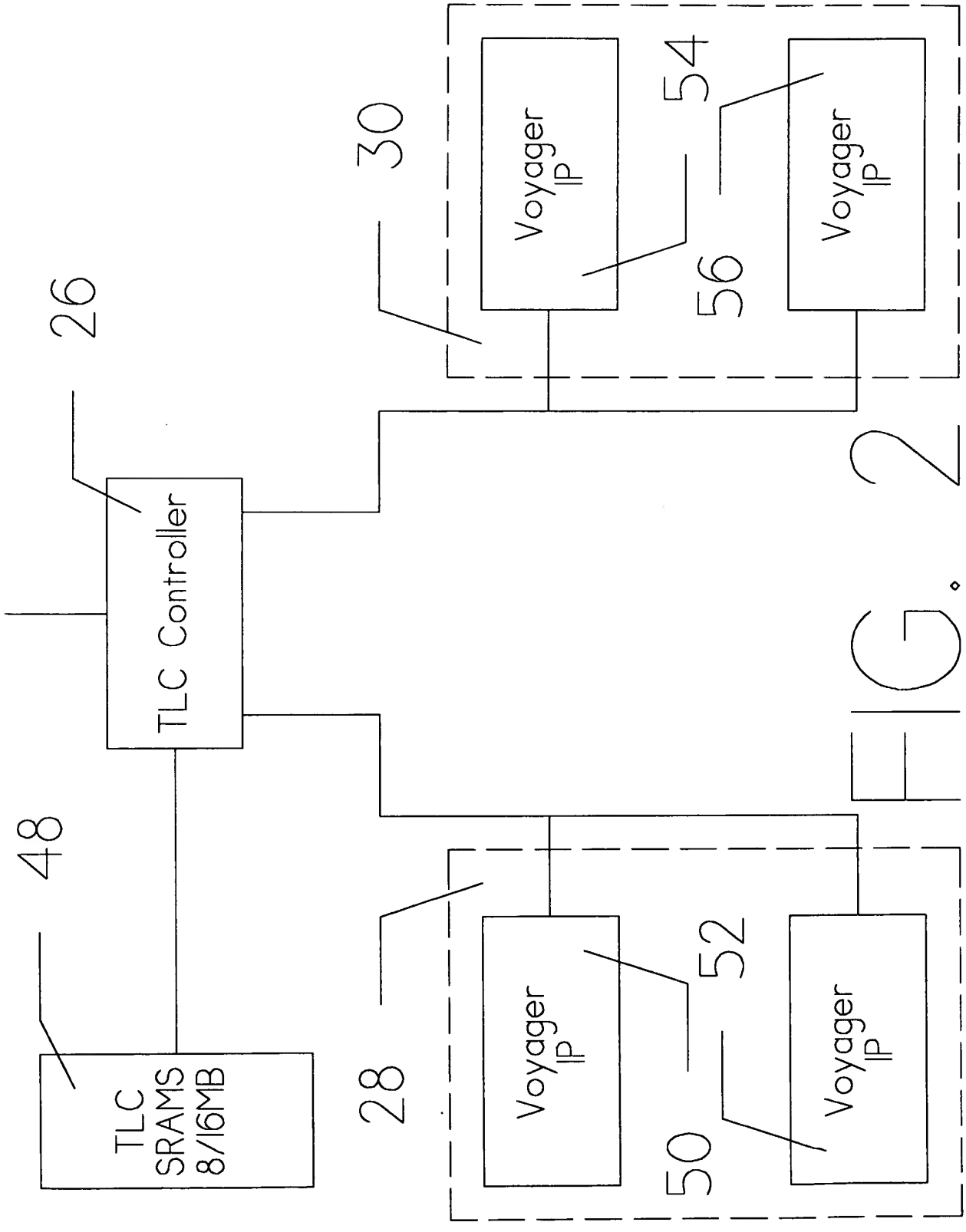


FIG. 2

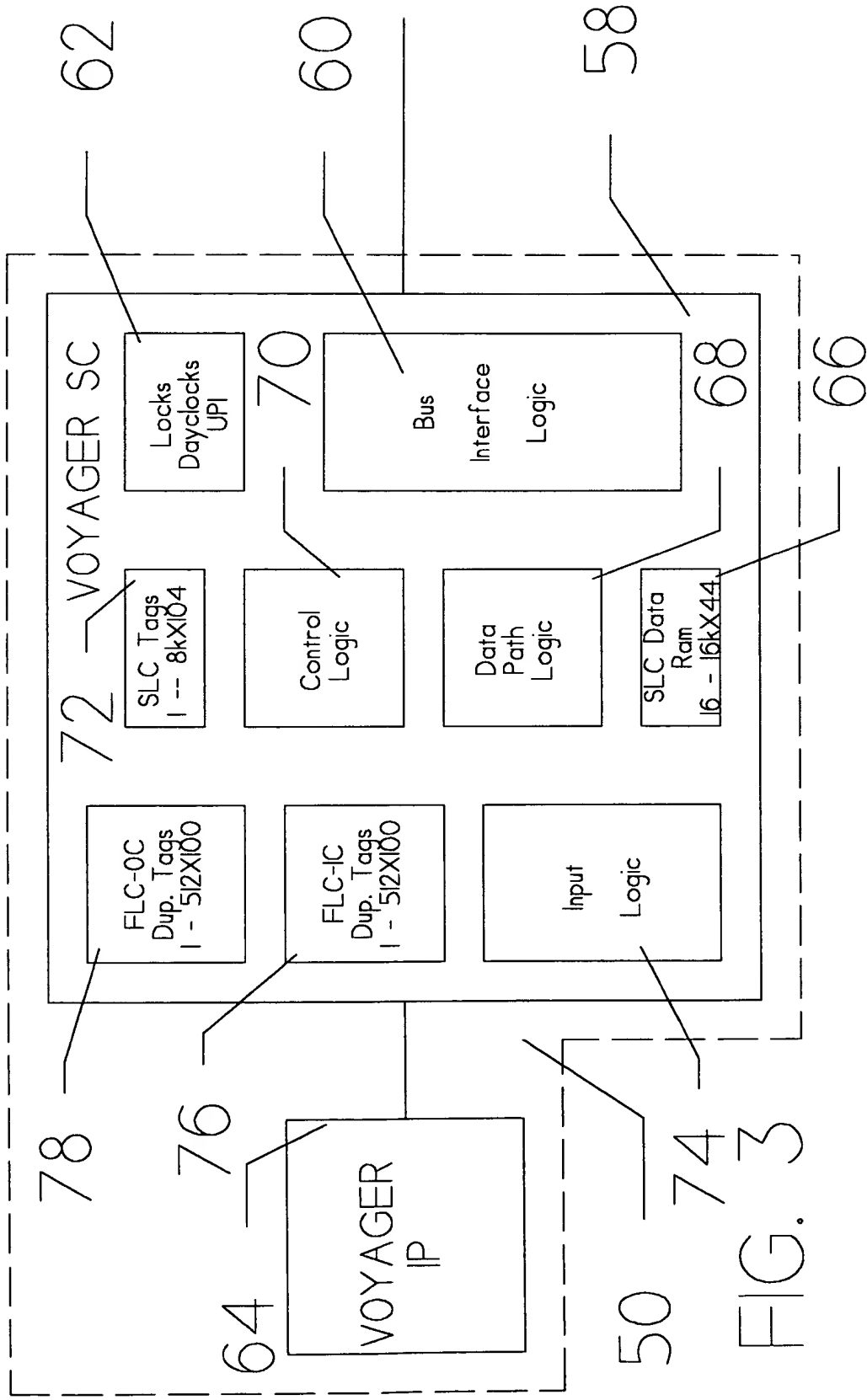
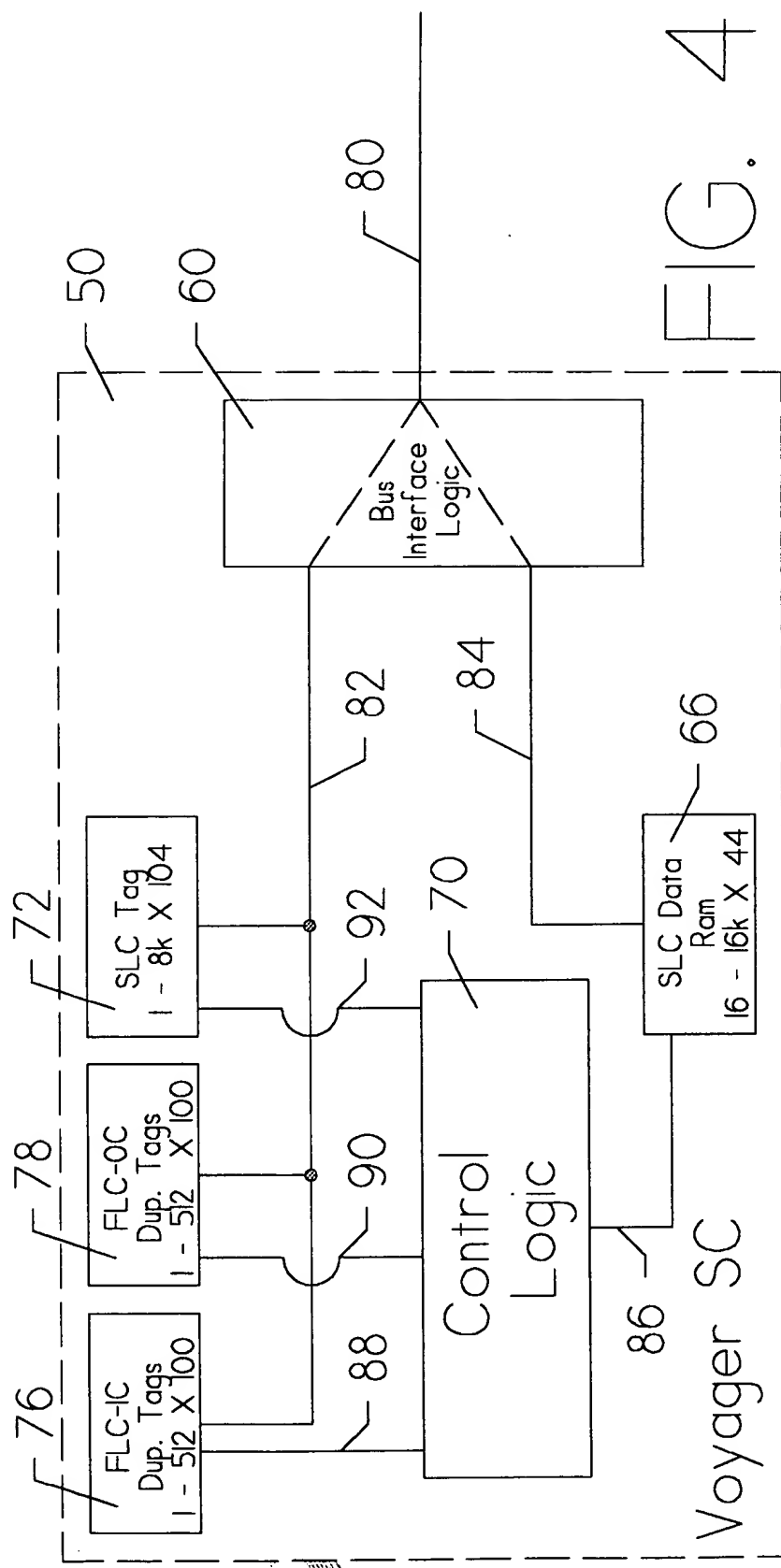


FIG. 3



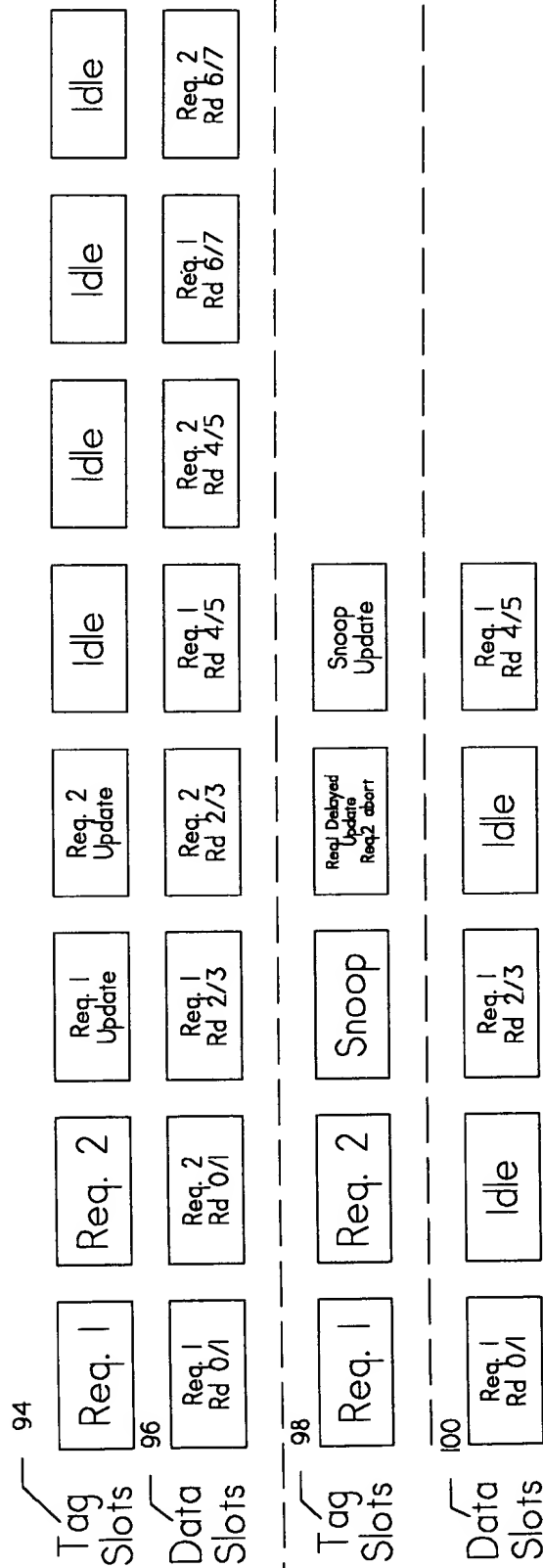


FIG. 5